USB3 Vision – FPGA Core

USB3 Vision® – compliant IP Core for FPGAs

USB3 Vision® is a standardized communication protocol for vision applications based on the widely used USB cables. It allows easy interfacing between cameras and PCs, because the protocol is well defined and supports GeniCam™ software standard.

Sensor to Image offers a set of IP cores and a development frame-work to build FPGA-based products with U3V interface.

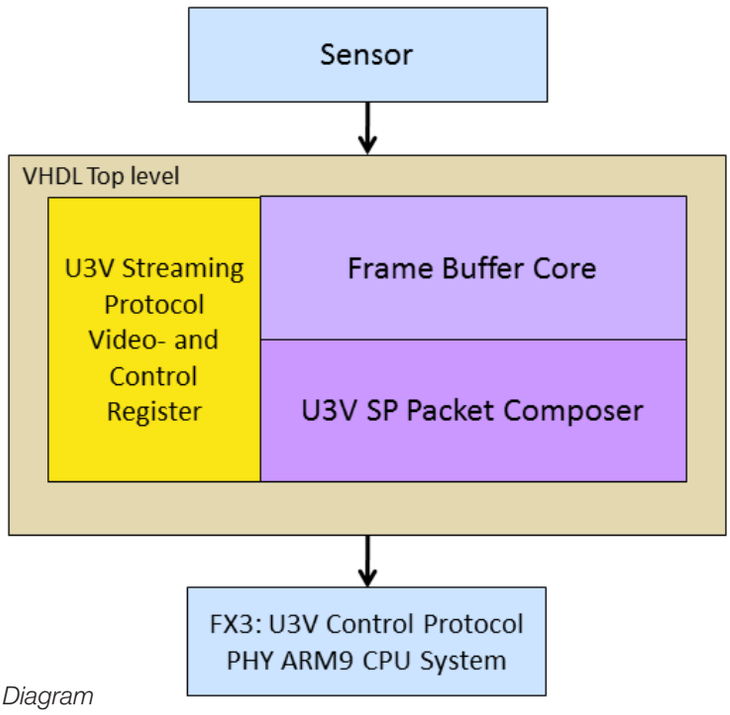
Due to the speed of U3V, a sender as a receiver needs a fast implementation in an FPGA with preferable embedded USB Core inside the FPGA. This core is available up from Spartan 6 or Cyclone IV devices. Our core is small enough that it leaves enough space for your application even using the smallest device out of these families.

The U3V FPGA solution is delivered as a reference design with FPGA IP cores, which allows a maximum in performance at a small footprint and enough flexibility to realize your custom solutions.

The following components are part of the design:

Top Level Design, which builds the interface between real hardware (e.g. sensor, CPU, U3V physical) and internal data processing. This module is delivered in source-code (VHDL), so it can be adapted and extended to custom hardware.

The U3VSP Streaming Interface takes all data from the video sensor to the U3V Core. It realizes the full speed on the Streaming Channel according to the U3V-specification.

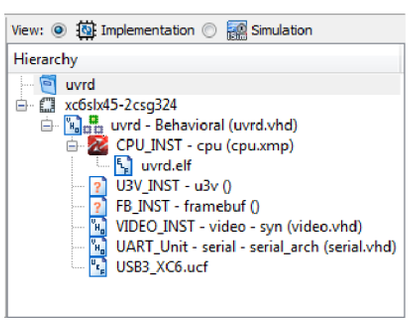


Block Diagram U3V Design

This modules provides set of basic registers required for a USB3 Vision camera. Additionaly it converts video data stream from an image sensor to the format required by the USB3 PHY.

The U3VCP Control Interface receives and sends all data from U3V HOST controll channel to the U3V Core and realizes the control channel according to the U3V-specification.

Cypress FX3 with integrated ARM CPU and physical interface is used to handle all USB 3 initialisation routines and USB3 Vision control channel. Some software parts are delivered as compiled files only (e.g. U3V-bootloader, U3V-controller), other parts are in source code. The delivered design framework comes with all necessary design files and cores, FPGA vendor tools project files and a U3V camera system with a CMOS imager. This system should be used as reference design and evaluation board. As development environment the XILINX, LATTICE or ALTERA development tools are used (not in scope of delivery).



ISE Project Tree

Available Modules

Module	Comment	LATTICE FPGA	ALTERA FPGA	XILINX FPGA
Sync. bus as sensor interface	incl. 1 single tap sensor adaption incl. I²C/SPI core + C code	•	•	•
U3V Core project licence	packet composer, PHY interface	•	•	•
XML-File generation	XML-File generation	•	•	•
Full sources, design, …	on request	•	•	•

other FPGA vendors on request

U3V Device Core

Module	Spartan 6	Artix 7	Cyclone V	ECP III
C3V Device Core				
– Slice registers	3134	3134	3204	4847
– Slice lookup tables	3161	3161	5252	3893
– Block RAMs	7	7	35	10
– Maximum clock frequency	117 MHz	177 MHz	118MHz	115MHz

values are post synthesize only and based on platform specific reference designs, other architectures might have different resource usage

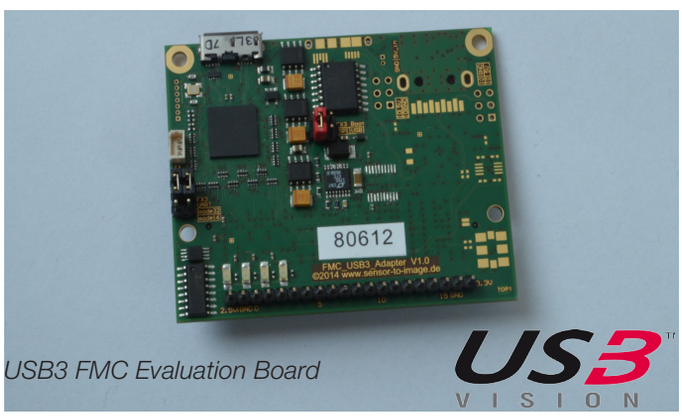
OPERATING SYSTEMS

MODULE	WIN 7/8	UBUNTU 12.04	CENTOS 6
Sphinx Library (.dll/.a)	•	•	•
USB3 Vision Driver	•	•	•
Sphinx U3V Viewer	•	•	•

SOURCE CODE

MODULE	STANDARD EDITION	COMMUNITY EDITION
Sphinx Library (.dll/.a)		•*
USB3 Vision Driver		•*
Sphinx U3V Viewer	•	•

* Ownership of U3V specification required



USB3 FMC Evaluation Board

TECHNOLOGY

Sensor to Image GmbH · Lechtorstraße 20 · D-86956 Schongau · Germany
Phone: +49 88 61-23 69-0 · Fax: +49 88 61-23 69-69 · email@sensor-to-image.de